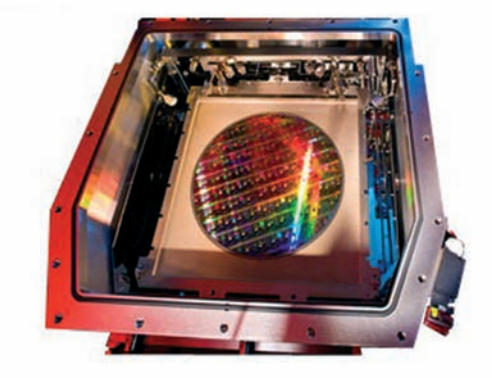
PROJECT RESULT

Technology platform
for process options

MEDEA+

2T210: Materials for next-generation capacitors and memories (MaxCaps)



Building high capacitance into chip memories

Integrating passive components such as resistors and capacitors into electronic circuitry has usually implied mounting them as discrete devices onto printed-circuit boards. The difficulties for circuit designers in coupling such external devices to sophisticated processing chips can be extreme. The MEDEA+ MaxCaps project aimed to solve this problem for capacitors by developing new materials and deposition methods that would make possible much higher capacitance levels within the chip itself. It succeeded, developing a dielectric value (k) of up to 100, a world first for DRAM memory packages.

Integration of passive devices into modern electronic circuitry presents a problem to designers seeking compact and powerful communications applications. It is little help building smaller and more efficient chip devices if the accompanying resistors and capacitors have to be mounted externally on the printed-circuit board (PCB).

The MEDEA+ 2T210 MaxCaps project focused on a key integration challenge: how to build more powerful passive devices, specifically capacitors, into system-on-chip (SoC) or system-in-package (SIP) designs. It aimed to develop new capacitor materials with a much higher dielectric constant (k) for computer memory applications. It sought a k value of up to 100, as opposed to the existing average of 20 to 40.

World first in k value

MaxCaps concentrated on two key areas for metal-insulator-metal (MIM) capacitor applications to develop improved precursors and atomic layer deposition (ALD) processes for:

1. The highest dielectric constant possible for integrated MIM capacitors in dynamic RAM (DRAM) and radio-frequency (RF) applications; and
2. Phase-change memory (PCRAM) which varies its resistivity according to the temperature applied – this emerging technology is seen as a promising candidate to replace embedded or stand-alone non-volatile memory.

As DRAM memory typically requires operating voltages of 1 V or less, low leakage targets, and hence larger k values, are easier to achieve than in higher voltage designs. MaxCaps achieved a k value of up to 100 with the smallest dielectric thickness and low leakage, a world first for DRAM and a significant step forward on the roadmap to the next generation of DRAM capacitors. This dielectric constant level was a headline achievement and was possible with the slimmest metal-oxide-based equivalent effective oxide thickness for a specified leakage current.

For integrated and interposed RF and blocking applications, which typically have operating voltages of up to 5 V, MaxCaps achieved an improvement of up to k equals 50, the highest value possible while keeping leakage current within sustainable limits. However, for capacitors with operating voltages of 30 to 100 V, while the project paved the way for further developments, it showed that it is very unlikely that any new materials could be developed to meet specifications for 100 V applications.

ALD a workable method

For the use in capacitors in particular, MaxCaps developed ALD and atomic vapour deposition (AVD®) for the complex-oxide dielectrics

$(Ba)SrTiO_3$ and $(Ba)SrTiO_3/Al_2O_3$ in multilayer structures, and managed to achieve k values greater than 50 on a TaN electrode layer, with good leakage current performance.

In the second major focus, improved materials for phase-change memory technologies, MaxCaps was able to develop the first $Ge_2Sb_2Te_5$-based memory cells using atomic layer deposition. The results indicate that with ALD technology becoming a workable approach to the reliable coating of complex 3D structures, the consequence for future designs will be a significant shrinking of cell footprint. Using ALD also solves the problem of how to heat the cells to achieve switching temperature. The smaller cell footprint made possible by ALD means less power is required for operation than in conventional cells.

Many of the advances achieved were only possible because of the successful adaptation of deposition tools and the development of new chemical precursors. MaxCaps was able to develop and test a number of key chemical precursors which yielded high-quality films.

Significant design benefits

The project results are highly significant for circuit designers. To go from planar devices such as discrete capacitors to trench capacitance within a CMOS chip delivers an increase in usable area of one to two orders of magnitude, making possible much higher capacitance levels from smaller footprint packages.

For major chipmakers Infineon, IPDiA and STMicroelectronics, the new technologies enable them to take the next step on the roadmap to more integrated capacitance in circuit designs. Some optimisation is still needed, but reaching where it is today would not have been possible without the achievements within the MEDEA+ project. MaxCaps has been a very important enabler in moving to the next generation of applications.

Partner Continental – a large-scale producer of automotive electronics – acknowledges that being able to supply high capacitance needs within the chip package, rather than externally, brings obvious benefits for PCB and surface-mount device manufacturing. Continental is already applying knowledge gained in MaxCaps to new industrial applications.

Across the industrial value chain

For the MaxCaps partners, the key advantage of MEDEA+ project participation was the involvement of actors throughout the industrial value chain – from chemical manufacturing to chip production. Those involved included chemical-precursor suppliers such as Air Liquide and SAFC HighTech, deposition tool manufacturers like ASM and Aixtron, and universities.

This interdisciplinary involvement of scientists and engineers from across industry enabled the project to reach its k-value target and develop atomic layer deposition as a workable solution for the next generation of memory packages.

No less important was the level of co-operation and openness achieved within the consortium, that helped avoid duplication of effort and enabled partners from widely differing industries to make progress. A well-defined project, good fit between partners and a good attitude were all pointed to as key ingredients in the project mix.

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PARTNERS:

Air Liquide
Aixtron
Analog Devices
ASM International
Bronkhorst
CEA-LETI
Continental
IHP
IMEC
Infineon Technologies
IPDiA
NXP Semiconductors
Oxford Instruments
R3T
SAFC Hitech
STMicroelectronics
Tyndall National Institute
Uni Eindhoven (TU/e)
Uni Helsinki

PROJECT LEADER:

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KEY PROJECT DATES:

Start: January 2008
End: August 2011

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The Netherlands
United Kingdom

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.